

Optimized Core for 32-bit Microcontroller and Embedded applications

Baseline Specifications

Product	MIPS32 M4K core
Process	130nm
Frequency (MHz) (worst case)	100 - 228
Max. Performance (DMIPS)	369
Power (mW/MHz) (Typical)	0.07 - 0.21
Core area (mm ²)	0.19 - 0.64

Product	MIPS32 M4K core
Process	90nm
Frequency (MHz) (worst case)	200 - 414
Max. Performance (DMIPS)	671
Power (mW/MHz) (Typical)	0.04 - 0.15
Core area (mm ²)	0.12 - 0.53

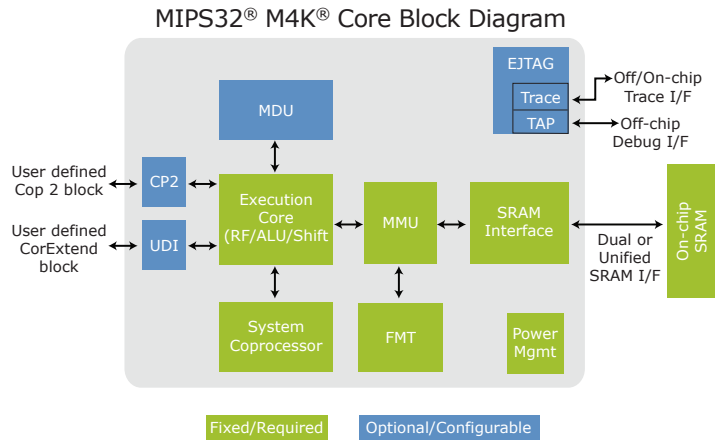
Note:

Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries. For 130nm, Worst case is slow silicon, 1.08V, 125C; Typical case is typical silicon, 1.2V, 25C. For 90nm, Worst case is slow silicon, 0.9V, 125C, Typical case is typical silicon, 1.0V, 25C.

Quoted speeds don't contain OCV, clock jitter and design margin.

MIPS32® M4K®

The MIPS32® M4K® core sets a new standard for 32-bit synthesizable cores. Optimized for embedded designs and controller applications, it features high frequency, small die area and very low power consumption. A wide range of configurable features allow designers to optimize the core's performance while reducing die size, power consumption and total system cost.



MIPS32 M4K Core Highlights

- Using the 5-stage pipeline, the M4K core offers more than 400MHz in frequency and greater than 1.5 DMIPS/MHz in performance.
- The M4K core has a build-time configurable external SRAM interface optimized for cacheless operation, enabling increased system performance and deterministic operation.
- The M4K core has built-in architectural features that enable reduced power consumption without effecting the frequency or performance.
- CorExtend™ capabilities enable designers to create highly-differentiated SoC designs by adding their own instructions.
- The highly-configurable and synthesizable core enables flexibility for designers to include only those features necessary for their application.
- A rich environment of software and hardware tools support ease of design and verification.
- MIPS16e™ code compression allows designers to reduce the memory requirements for their applications by as much as 40%.
- BIST, scan and Enhanced JTAG (EJTAG) debug with trace (PDtrace™ and iFlowtrace™) and fast download enable quick and easy debugging.

Key Applications:

- Digital home: DTV, MoCA-based subsystems for cable modems, Set-top Boxes (STBs), and Residential Gateway (RG)
- 32-bit Microcontrollers: Automotive and Industrial control systems
- Portable devices: Digital camera, GPS receivers, MP3 players, and Mobile broadband applications
- Wireless networking: Bluetooth, UWB, and Wireless HD multimedia

Features

MIPS32®-enhanced (Release 2) architecture

- 5-stage pipeline
- 1, 2, 4 or 8 sets of thirty-two 32-bit general-purpose registers
- Memory management unit with simple fixed mapping translation (FMT)
- Bit field manipulation instructions
- Vectored interrupts and support for external interrupt controller
- Atomic interrupt enable/disable

User-defined instruction-set add (CorExtend™) extensions

- Maintains full MIPS32 compatibility
- Supported by industry-standard development tools
- Single- or multi-cycle instructions

MIPS16e™ code compression

- 16-bit encodings of 32-bit instructions to improve by as much as 40%
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines

SRAM interface

- Single- or multi-cycle transaction latency
- Support for semaphores to control access to shared resources
- Separate or unified instruction and data memory interface

Multi-core support

- External lock indicator enables multi-processor semaphores
- External sync indicator allows memory ordering

Integer multiply/divide unit (MDU)

- Fast or area-efficient, configurable at build time
- Maximum issue rate of one 32x16 multiply per clock (fast MDU)
- Maximum issue rate of one 32x32 multiply every other clock (fast MDU)

General purpose coprocessor (COP2) interface

- 32-bit interface to an external coprocessor

Power control

- Minimum frequency: 0 MHz
- Power-down mode (triggered by WAIT instruction)
- Support for software-controlled clock divider
- Support for extensive use of local gated clocks

EJTAG debug

- Support for single stepping
- Complex breakpoints and triggers, configurable at build time
- PC and data tracing (PDtrace™)
- iFlowtrace™ mechanism for instruction addresses - compact trace block and efficient trace compression
- Cross-CPU breakpoint support

Development tools

- MIPS SDE – GNU based toolchain optimized to support MIPS cores
- MIPSsim™ – Bus-functional modeling and instruction set simulator
- System Navigator™ probe – EJTAG probe
- NavigatorIDE – Eclipse-based graphical integrated development environment

Exceptional performance
density and design flexibility
for microcontrollers,
networking and wireless
applications

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